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1 (Canceled)

2 A dynamically reconfigurable VLSI device for implementing in hardware any multiple outputs combinational target circuit having the output functions expressed in logical sum-of-product equations with a maximum of m inputs, a maximum of r outputs and a maximum of n product terms p(k), comprising:

a register with m bits for storing the input variables;

n cells, a cell C(k) for determining the logical value of a product term p(k) of said equations for given inputs;

a block of r OR gates, each one with n inputs, associated with said cells C(k) for receiving the logical value of product terms p(k) and outputting the r bits of output functions;

wherein said cell C(k) comprises:

a storage area for storing the information that characterizes a product term, named mask word, product word and function word;

first logic level means for receiving said m inputs and said mask word to produce a first intermediate result, which identify the input variables that form a product term;

second logic level means for comparing the said product term with said first intermediate result to produce a second intermediate result concerning a product term;

third logic level means for receiving said second intermediate result to produce the logical value of the product term; and

forth logic level means for transferring said function word to r outputs, according to said logical value of said product term p(k), and subsequently to be OR-ed with function words of other product terms.

3 A dynamically reconfigurable VLSI device as in claim **2**, wherein said storage area of a cell C(k) comprises two m-bit registers and one r-bit register.

4 A dynamically reconfigurable VLSI device as in claim **2**, wherein said first logic level of a cell C(k) comprises m*(2-bit) AND gates, each one for receiving a respective bit of said m input variables and of said mask word to produce said first intermediate result.

5 A dynamically reconfigurable VLSI device as in claim **2**, wherein said second logic level of a cell C(k) comprises m*(2-bit) XNOR gates, each one for receiving a respective bit of said first intermediate result and of said product word to produce a bit of said second intermediate result.

6 A dynamically reconfigurable VLSI device as in claim **2**, wherein said third logic level of a cell C(k) comprises one m-bit AND gate to produce a logical value which is the value of the product term.

7 A dynamically reconfigurable VLSI device as in claim **2**, wherein said forth logic level of a cell C(k) comprises m*(2-bit) AND gates for transferring said function word to outputs, considering the logical value of said product term p(k).

8. (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware a target synchronous sequential circuit with maximum 2^s states, clock input only and outputs taken from the state register, wherein the multiple outputs combinational circuit which establish the next state defined by

sum-of-product logical equations is implemented according to claim **2**, with maximum *s* inputs, maximum s outputs and maximum n product terms p(k) and wherein the input register is a state register with s bits; and further comprising:

a feedback connection to establish the next state.

9. (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware a target synchronous sequential circuit with maximum 2^s states, m data inputs, clock input and r outputs, wherein two multiple outputs combinational circuits are implemented according to claim **2**, the first combinational circuit defined by the next state sum-of-product logical equations with maximum (m + s) inputs, maximum s outputs and maximum n1 product terms p(k) and the second combinational circuit defined by the output sum-of-product logical equations, with maximum s inputs, maximum r outputs, and maximum n2 product terms p(k); and further comprising:

a state register with s bits, wherein said state register is the input register of the second combinational circuit;

a feedback connection to establish the next state.

10 (Canceled)

11 (Canceled)

12 A dynamically reconfigurable VLSI device for implementing in hardware any multiple-output combinational target circuit defined by a group of logical sum-of-product equations, with maximum m inputs, maximum r outputs and a maximum of q product terms in each equation, having a register with m bits for storing the input variables and for each single sum-of-products logical equation, considered as an independent equation, further comprising:

q modified cells, a modified cell C(k) for determining the logical value of a product term p(k) of said independent equation, for given inputs;

a single OR gate associated with said q modified cell C(k) for receiving the logical value of product terms p(k) to provide a single output for said independent equation;

wherein said modified cell C(k) comprises:

a storage area formed by two m-bit registers for storing the information that characterizes a product term, named mask word and product word;

first logic level that comprises m*(2-bit) AND gates, each one for receiving a respective bit of said inputs and of said mask word to produce a respective bit of first intermediate result, which identify the input variables that form a product term;

second logic level that comprises m*(2-bit) XNOR gates, each one for receiving a respective bit of said product word and said first intermediate result to produce a second intermediate result concerning a product term; and

third logic level that comprises one m-bit AND gate for receiving the m bits of said second intermediate result to produce a logical value which is the value of the product term.

13. (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware a target synchronous sequential circuit with maximum 2^s states, clock input only and outputs taken from the state register, wherein the multiple outputs combinational circuit which establish the next state defined by sum-of-product logical equations is implemented according to claim **12**, with maximum *s* inputs, maximum s outputs and maximum q product terms p(k) in each said equation and wherein the input register is a state register with s bits; and further comprising:

a feedback connection to establish the next state.

14. (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware a target synchronous sequential circuit with maximum 2^s states, m data inputs, clock input and r outputs, wherein two multiple outputs combinational circuits are implemented according to claim **12**, the first

combinational circuit defined by the next state sum-of-product logical equations with maximum (m + s) inputs, maximum s outputs and maximum q1 product terms p(k) in each said next state equation, and the second combinational circuit defined by the output sum-of-product logical equations, with maximum s inputs, maximum r outputs and maximum q2 product terms p(k) in each said output equation; and further comprising:

a state register with s bits, wherein said state register is the input register of the second combinational circuit;

a feedback connection to establish the next state.

15 (Currently amended) A method for implementing target circuits selected from multiple-output combinational circuits and from synchronous sequential circuits, having their behavior described by groups of logical sum-of-product equations, wherein each said group of logical sum-of-product equations is implemented in a dynamically reconfigurable VLSI device, as in claims **2** or **12**, the method comprising the steps of:

inputting a request to reconfigure said VLSI device to said target circuit;

identifying the VLSI device to be configured, considering its internal structure, of type cell C(k) or of type modified cell C(k);

generating memory words uniquely defining each product term p(k) of said sum-of-products logical equations; and

implementing the target circuit by storing said memory words into a corresponding registers of type cell C(k) or of type modified cell C(k).